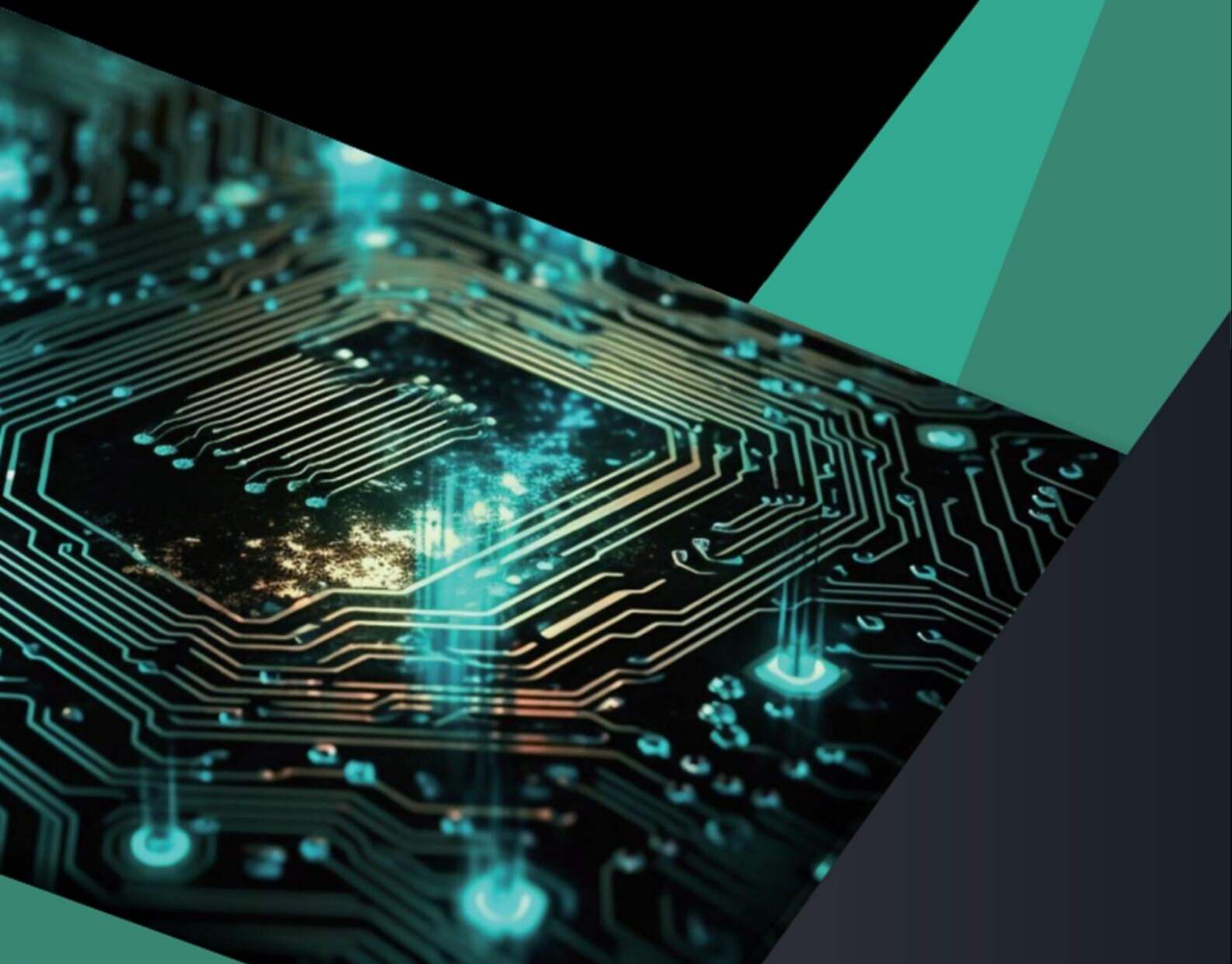


January 2026

AI-Driven Memory Supercycle: 2025-2027 Strategic Outlook

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About Brioccean

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At Brioccean, quality is our cornerstone. Our commitment is to ensure that every component we source is of the highest quality.

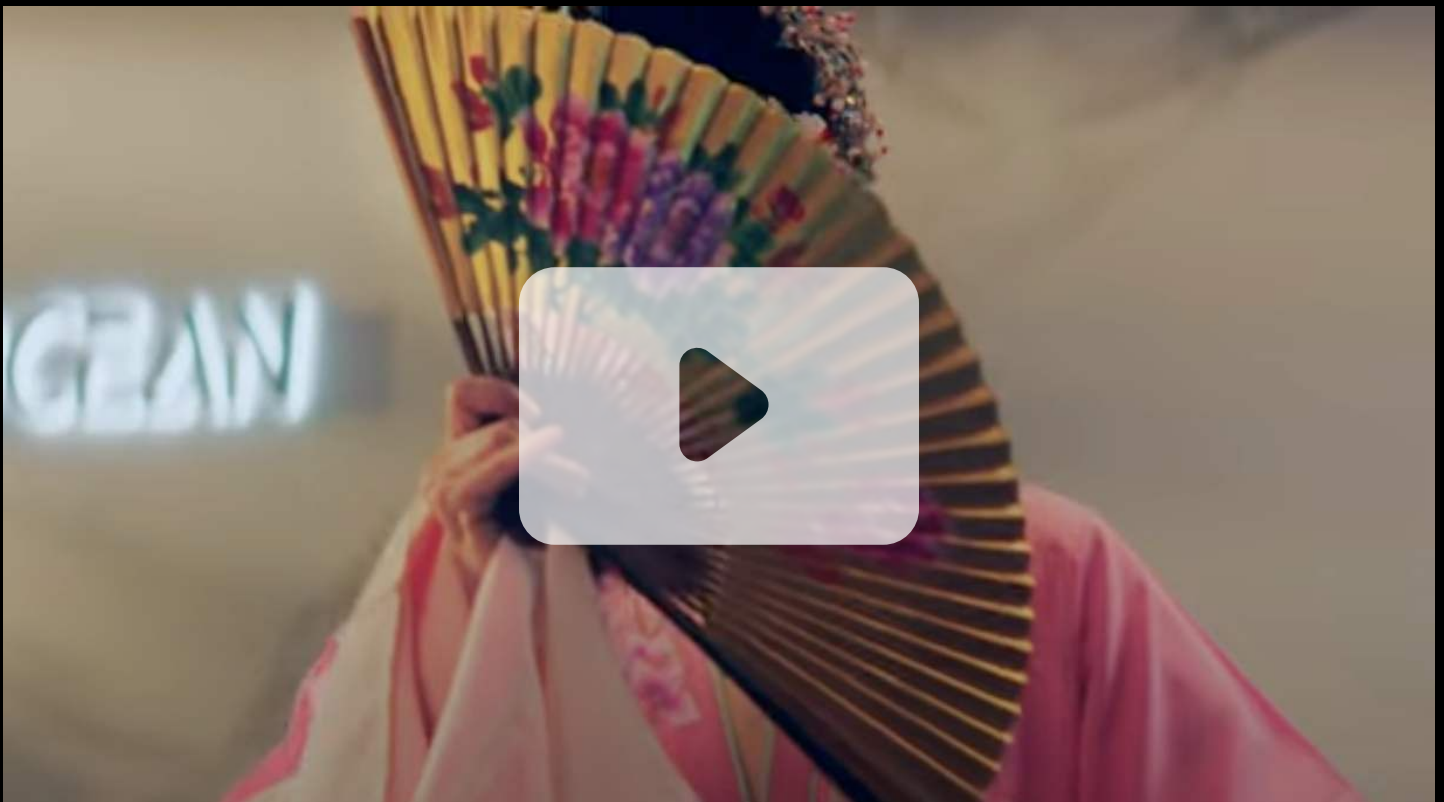


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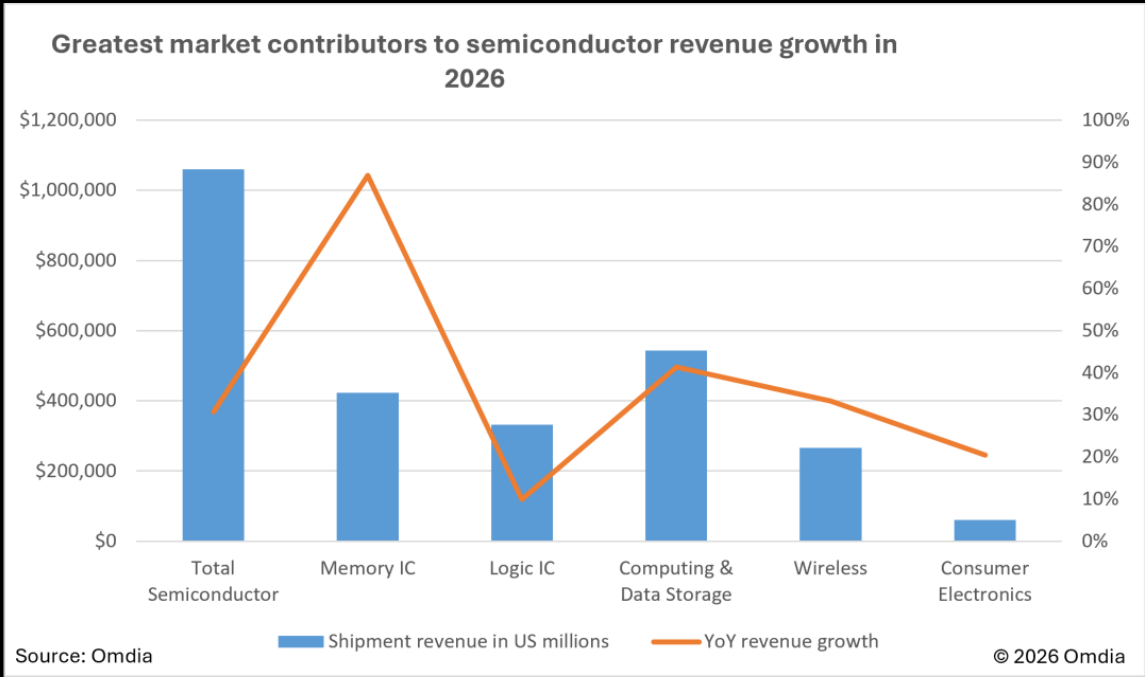
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Executive Summary

The global semiconductor memory market is undergoing a historic, memory-led supercycle, with scale and intensity surpassing earlier forecasts. Omdia projects the total semiconductor market will surpass \$1 trillion in revenue in 2026, with the Memory IC segment itself forecast to grow by 85-90%.

Figure 1: Greatest Market Contributors to Semiconductor Revenue Growth in 2026



Source: Omdia

This is driven by a severe structural supply-demand imbalance, primarily fueled by AI's explosive demand for High Bandwidth Memory (HBM) and high-density server DRAM, which collides with strategically constrained supply as manufacturers prioritize HBM capacity.

This imbalance has triggered dramatic price surges across all segments. Data from TrendForce indicates DRAM and NAND Flash contract prices are forecast to rise 55-60% QoQ in Q1 2026. The spot market distortion is most acute, with legacy DDR4 prices rising from approximately \$7 in mid-2025 to over \$78 by January 2026.

Consequently, a foundational power shift has occurred: suppliers hold decisive pricing authority, traditional quarterly negotiations have dissolved, and a prolonged allocation-based model is entrenched. With a supply-demand balance not expected before H1 2027, a strategic paradigm shift from cost-optimized procurement to securing long-term capacity and building resilient supply chains is now imperative.

01

Macro Trends Shaping the Global Storage Landscape

1. Macro Trends Shaping the Global Storage Landscape

1.1 Demand Inflection: AI as the New Structural Baseline

Demand is being redefined by the exponential requirements of generative AI workloads, which are transitioning from model training to inference—a phase requiring vast, sustained data throughput. This shift creates a permanent new baseline of demand that extends beyond traditional cycles, compelling hyperscale cloud providers (CSPs) to lock in long-term supply. The specifications for NVIDIA's Vera Rubin platform, entering mass production, illustrate this inflection point. Each Rubin GPU will be configured with 288GB of HBM4, while the companion Vera CPU will support up to 1.5TB of LPDDR5X memory, setting a new benchmark for system memory that dwarfs previous generations.

This demand is not isolated to high-performance memory. AI inference also drives a structural upgrade in storage architecture, accelerating the adoption of high-capacity, cost-optimized QLC-based Enterprise SSDs to handle petabyte-scale AI data lakes. Consequently, the industry is witnessing a multi-vector demand shock: while HBM and server DRAM feed the GPU, high-density NAND serves the data pipeline, creating simultaneous, inelastic pressure across all storage segments.

1.2 Supply-Side Recalibration: The Strategy of Deliberate Scarcity

Supply growth is strategically constrained and structurally incapable of keeping pace with this new demand curve. The cornerstone of this constraint is the deliberate reallocation of wafer capacity towards high-margin products. The industry faces a severe “bit penalty” in High Bandwidth Memory (HBM) production, where manufacturing 1GB of HBM consumes the equivalent silicon wafer area of 2-3GB of standard DRAM, actively reducing the total available output for conventional products.

This reallocation is being compounded by active supply management in the NAND market. Recent industry reports confirm that Samsung and SK Hynix—collectively controlling over 60% of global NAND production—are planning to reduce their NAND wafer input in 2026. Specifically, Samsung's input is forecast to drop from 4.90 million units in 2025 to 4.68 million units, and SK Hynix's from 1.90 million to 1.70 million units. This calculated supply reduction, driven by a focus on profitability over market share, decisively tightens the market.

Major capital expenditure plans from top manufacturers like Samsung, SK Hynix, and Micron are oriented towards HBM and next-generation DRAM, with new greenfield fabs not expected to deliver material new capacity until 2028 at the earliest. This locks in a prolonged period of structural undersupply for 2026-2027.

1.3 Pricing Power and Market Conduct: Quantifying the Imbalance

The structural supply-demand mismatch has decisively shifted pricing power to memory suppliers, leading to a breakdown of traditional quarterly negotiation mechanisms. As of January 2026, price increases are intensifying and broadening across product categories.

Current forecasts project significant price growth for Q1 2026. TrendForce estimates DRAM contract prices will rise by 55%-60% quarter-over-quarter (QoQ), with server DRAM exceeding 60% QoQ. NAND Flash contract prices are forecast to increase by 33%-38% QoQ, with client SSD prices rising over 40% QoQ.

This environment has prompted unprecedented supplier conduct. Major manufacturers have shifted to allocation-based models and, in some cases, suspended forward price quotations. These actions reflect a market where securing supply allocation has become a primary challenge, surpassing traditional price negotiations.

The supply crunch, driven by capacity reallocation to advanced products, has created acute shortages in legacy segments. This is most evident in the spot market for DDR4 memory. Industry analysis indicates DDR4 prices have increased substantially, with reports of spot prices for modules rising approximately 1800% from late 2024 to December 2025. The shortage has led to DDR4 spot prices sustaining a premium over DDR5, an inversion of traditional generational pricing. The tightness is expected to persist, with DDR4 contract prices forecast to rise up to 50% in Q1 2026.

Figure 1-1: Forecasted Memory Contract Price Trends (2025-2026)

QoQ %	1Q25	2Q25	3Q25	4Q25E	1Q26F	2Q26F	3Q26F	4Q26F
PC DRAM	DOR4: down 12~15% DOR5: down 10~15% Blended: down 10~15%	DOR4: up 12~15% DOR5: up 3~8% Blended: up 3~8%	DOR4: up 38~43% DOR5: up 3~8% Blended: up 3~15%	DOR4: up 49~45% DOR5: up 55~45% Blended: up 53~45%	DOR4: up 65~70% DOR5: up 50~55% Blended: up 50~55%	DOR4: up 10~15% DOR5: up 10~15% Blended: up 10~15%	up 3~8%	up 0~5%
Server DRAM	DOR4: down 10~15% DOR5: down 3~8% Blended: down 5~10%	DOR4: up 18~23% DOR5: up 3~8% Blended: up 3~8%	DOR4: up 28~33% DOR5: up 3~8% Blended: up 3~8%	DOR4: up 60~65% DOR5: up 53~58% Blended: up 53~55%	DOR4: up 65~70% DOR5: up 60~65% Blended: up 60~65%	DOR4: up 10~15% DOR5: up 10~15% Blended: up 10~15%	up 3~8%	up 0~5%
Mobile DRAM	LPOORAX: down 8~13% LPOORSX: down 3~8%	LPOORAX: up 0~5% LPOORSX: up 3~8%	LPOORAX: up 38~43% LPOORSX: up 10~15%	LPOORAX: up 48~53% LPOORSX: up 43~48%	LPOORAX: up 45~50% LPOORSX: up 43~50%	LPOORAX: up 10~15% LPOORSX: up 18~23%	LPOORAX: mostly flat LPOORSX: up 13~15%	LPOORAX: mostly flat LPOORSX: up 5~10%
Graphics DRAM	GOOR6: down 5~13% GOOR7: down 0~5%	GOOR6: mostly flat GOOR7: down 0~5%	GOOR6: up 22~25% GOOR7: up 5~10%	GOOR6: up 25~30% GOOR7: up 30~55%	GOOR6: up 45~50% GOOR7: up 45~50%	GOOR6: up 0~5% GOOR7: up 5~15%	GOOR6: up 0~5% GOOR7: up 3~5%	GOOR6: mostly flat GOOR7: up 0~5%
Consumer DRAM	DOR3: down 3~8% DOR4: down 10~15%	DOR3: mostly flat DOR4: up 15~23%	DOR3: up 50~60% DOR4: up 85~90%	DOR3: up 55~60% DOR4: up 35~50%	DOR3: up 45~50% DOR4: up 45~50%	DOR3: up 3~5% DOR4: up 3~5%	DOR3: up 0~5% DOR4: up 0~5%	DOR3: mostly flat DOR4: mostly flat
Total DRAM	Conventional DRAM: down 5~15% HBM Blended: down 0~5% (HBM Penetration: 5%)	Conventional DRAM: up 5~10% HBM Blended: up 5~10% (HBM Penetration: 9%)	Conventional DRAM: up 10~15% HBM Blended: up 15~20% (HBM Penetration: 8%)	Conventional DRAM: up 45~50% HBM Blended: up 50~55% (HBM Penetration: 12%)	Conventional DRAM: up 55~60% HBM Blended: up 50~55%	Conventional DRAM: up 13~15%	Conventional DRAM: up 3~5%	Conventional DRAM: up 0~5%

Source: TrendForce, Dec. 2025

Source: TrendForce

1.4 The Broader Milestone: A Memory-Led Super Cycle

This transformation is the central driver of a landmark event for the semiconductor industry. The sector is projected to surpass \$1 trillion in revenue for the first time in 2026, growing at 30.7% year-over-year. Crucially, this growth is highly concentrated: the Memory IC segment itself is forecast to expand by 85-90% in 2026. The explosive price increases detailed in section 1.3 are the direct mechanism fueling this historic expansion, irrefutably underscoring the current period as a definitive, memory-led super cycle where storage is not merely a participant but the principal engine of industry growth.

Industry consensus, as reflected in the latest analysis from TrendForce and major investment banks, projects that a balance between supply and demand is unlikely to be achieved before the first half of 2027. This extended timeline confirms the prolonged nature of the current seller's market.

In summary, the macro trend is defined by a seller's market of strategic creation. The confluence of inelastic AI demand, supplier-led capacity discipline, and structural production bottlenecks has reset the industry's fundamentals. This has established a prolonged period of tight supply, elevated and volatile pricing, and allocation-based commerce, challenging all participants in the electronics value chain to adapt their strategies for a new era.

02

DRAM & HBM Deep Dive – The Core Battleground

2. DRAM & HBM Deep Dive – The Core Battleground

The DRAM and HBM (High Bandwidth Memory) markets represent the epicenter of the AI-driven storage supercycle. Here, unprecedented demand for computational speed collides with the most severe structural supply constraints, creating the most volatile and strategically critical segment of the industry.

2.1 Conventional DRAM: Market Bifurcation and the DDR4 Paradox

The conventional DRAM market is undergoing a dramatic bifurcation, driven by the accelerated transition to AI-optimized platforms and the consequent neglect of legacy nodes.

DDR5 as the New AI Mainstream: The mass deployment of next-generation server platforms (Intel Granite Rapids, AMD Turin) is creating insatiable demand for high-density DDR5 modules. This demand is so intense that the profitability of server DDR5 is rapidly converging with, and is projected to surpass, that of HBM3e in the first half of 2026. This remarkable convergence fundamentally reshapes manufacturers' internal wafer allocation calculus, creating direct competition for capacity between these two high-margin segments. The price surge for DDR5 is historic and sustained, as quantified in the forecast below.

Table 1: DDR5 64GB RDIMM Contract Price Forecast & Drivers

Quarter	Price (USD)	QoQ Change	Market Driver
Q3 2025 (Actual)1	\$~255	Baseline	Upturn cycle commencement.
Q4 2025 (Actual)	\$450	+40% - +50%	Massive data center build-out by global CSPs; supplier pricing power at historic highs.
Q1 2026 (Forecast)	Expected to climb further to ~700	+40% - +50%	Surging demand from AI & data center servers; DRAM bit supply growth (~24% YoY in 2026) lags severely. Recovery in traditional server market (~50% DRAM demand growth YoY in 2026).
Q2 2026+	Stabilization at High Plateau	Increase expected to moderate to ~20%	Tight supply-demand dynamics continue. DDR5 profitability projected to surpass HBM3e from Q1 2026, complicating suppliers' capacity allocation decisions.

Source: TrendForce

The "Zombification" of DDR4: A stark paradox defines the legacy market. While the industry focuses on DDR5 and HBM, demand for DDR4 remains structurally vital across industrial, automotive, and cost-sensitive consumer applications. The accelerated exit of major manufacturers from this segment has created a severe supply vacuum. This has led to the extraordinary market distortion where DDR4 spot prices have consistently traded at a significant premium to DDR5, with reports indicating premiums as high as 48% in certain periods. This "scarcity paradox" transforms a legacy technology into a high-risk, high-cost component, forcing downstream industries into dependency on a shrinking pool of secondary suppliers.

2.2 HBM Market: The Apex of Technology and Allocation

HBM remains the highest-value and most constrained segment, representing the pinnacle of the AI memory demand curve.

Technology Transition to HBM4: The industry is advancing from HBM3e to HBM4, which features 16-high stacks and targets bandwidth over 2.0 TB/s. While SK Hynix has announced the first mass production system, yield challenges on advanced nodes may constrain the initial ramp, extending tight supply into 2026. HBM4 is expected to command a 30-40% price premium over HBM3e, reflecting its higher complexity and performance.

Sold-Out Capacity and Competitive Landscape: SK Hynix maintains a leadership position with an estimated 50-60% market share, bolstered by its deep partnership with TSMC for advanced packaging. Samsung is in an aggressive, resource-intensive catch-up mode, and Micron is rapidly scaling its output. The defining market feature is that effectively all 2026 capacity from major suppliers is pre-allocated to key AI accelerator vendors (NVIDIA, AMD, etc.) via LTAs, leaving no material spot market and creating an insurmountable barrier for new entrants.

The competition for the next-generation HBM4 is intensifying. Reports indicate Samsung's HBM4 has met key performance benchmarks, achieving a per-pin speed of 11 Gbps. The company aims to triple its HBM bit output in 2026, targeting a market share increase to over 35%, challenging SK Hynix's current leadership. To address the sold-out capacity, both giants are undertaking historic expansions. Samsung has commenced construction on a new \$41.5 billion fab (P5) in Pyeongtaek, while SK Hynix is accelerating its M15X fab and a major packaging facility in Indiana. These greenfield projects mean substantial new HBM capacity will only begin to come online in 2027-2028, underpinning the long-term structural shortage.

2.3 Cross-Product Dynamics and Profitability Convergence

A pivotal market trend is the convergence in profitability between server DDR5 and HBM (HBM3e/HBM4). This shift is driven by steep quarterly price increases for DDR5, coupled with a compression of the historical price premium for HBM. Industry analysis projects the price ratio between HBM and DDR5 to narrow to approximately 1.5-2x by late 2026, from a previously higher multiple.

This convergence impacts supplier capacity allocation decisions. Advanced wafer capacity must be allocated between the high-volume, high-margin DDR5 segment and the strategically critical HBM segment, which is tied to long-term agreements with key AI accelerator vendors. The competition for capacity between these two segments contributes to overall market tightness.

The ongoing transition to HBM4 and the development of DDR6/LPDDR6 are expected to influence future profitability dynamics and product roadmaps beyond 2026.

03

NAND Flash and Storage Technology Transformation

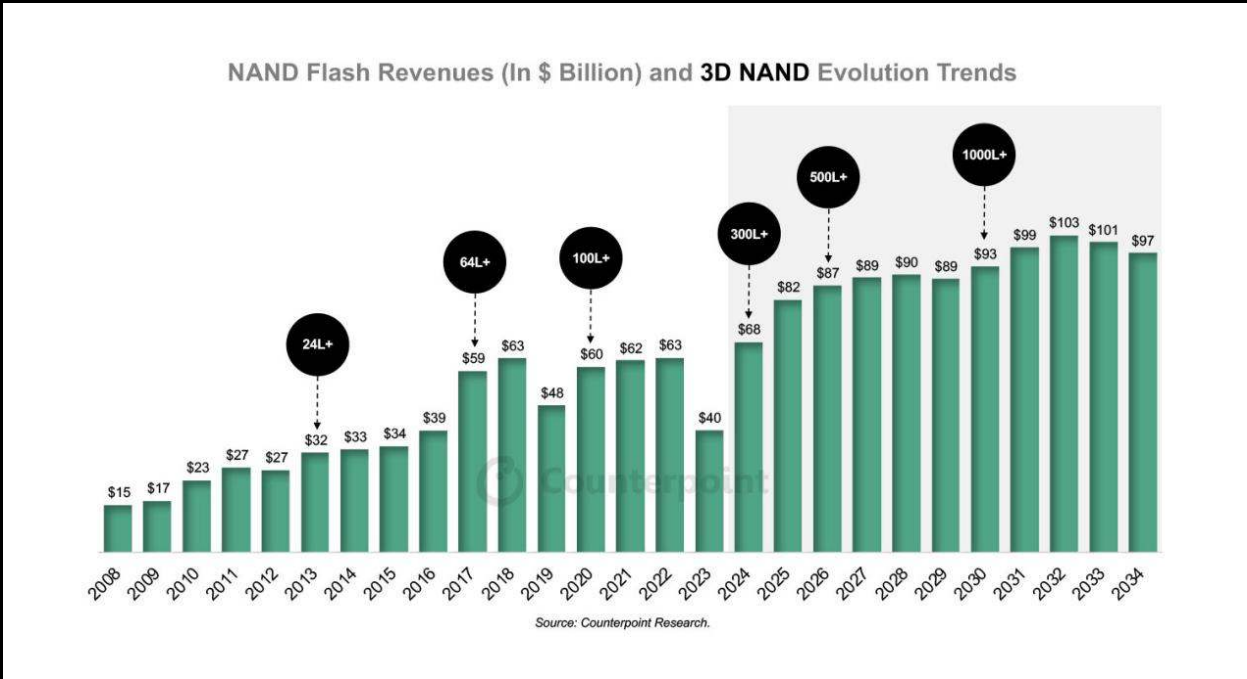
3. NAND Flash and Storage Technology Transformation

The NAND Flash market is experiencing a paradigm shift, transitioning from a historically cyclical commodity market to one driven by sustained, structural demand from AI and data-centric workloads. This transformation is characterized by a fundamental recalibration of supply dynamics, technology roadmaps, and competitive strategies.

3.1 Market Evolution: From Cyclicity to AI-Driven Structural Growth

The NAND Flash market is undergoing a historic paradigm shift, transitioning from a past defined by macroeconomic and consumer-driven cycles to a future shaped by structurally sustained, technology-fueled demand from AI. Figure 3-1: NAND Flash Revenues and 3D NAND Evolution Trends provides a long-term visualization of this transition, plotting revenue against pivotal 3D NAND layer breakthroughs.

Figure 3-1: NAND Flash Revenues and 3D NAND Evolution Trends



Source: Counterpoint Research

As illustrated, the pre-2025 market followed predictable cyclical patterns tied to consumer electronics. The period from 2025 onward marks a decisive divergence. The requirement for high-capacity AI storage, coinciding with the industry's crossover into 300+ layer production, has created a self-reinforcing cycle of value growth. This long-term view underscores the structural break initiated by AI.

This break is characterized by a new, inelastic demand baseline. The shift to multimodal AI has escalated storage needs, making high-capacity Enterprise SSDs (eSSDs) the core workhorse for AI data pipelines. Unlike past cycles, the current tightness is validated by historically low channel inventory levels (e.g., SSD inventory at approximately 8 weeks in early 2026) and sustained price increases, indicating a supply-constrained environment projected to persist.

The transition is further cemented by supply-side constraints. Leading manufacturers are exercising capital discipline, with NAND capital expenditure growth projected to be moderate in 2026 (industry analysts estimate an increase of about 5%), prioritizing technology migration over blanket capacity expansion. The industry's race to advance 3D NAND layer counts faces increasing complexity, particularly with the adoption of Hybrid Bonding, which raises the structural cost floor for advanced production.

This confluence of sustained AI demand, disciplined supply growth, and escalating technological complexity moves the NAND market into a new, technology-and-demand-driven growth paradigm targeting 500+ layers and beyond.

3.2 Explosive Growth of eSSD: The Engine of AI Data Pipelines

The forecasted revenue surge is fundamentally driven by the transformation of enterprise storage. AI workloads have created a new, inelastic demand curve.

Demand Catalyst: The AI training and inference cycle places unprecedented demands on storage infrastructure. Frequent model checkpointing requires immense, sustained write bandwidth, while querying massive data lakes demands high random read performance. This has led to explosive, structural demand for high-capacity QLC-based eSSDs (30TB-64TB), which offer the optimal \$/TB for petabyte-scale AI data repositories.

Compound Bottlenecks: Shortages extend beyond NAND flash wafers. The supply of advanced SSD controllers, particularly for PCIe Gen5/Gen6 interfaces, and other critical components like power management ICs, has become a second-layer bottleneck, capping total eSSD output and extending lead times.

3.3 Manufacturer Discipline: Strategic Supply Management for Sustained Profitability

Haunted by the severe losses of 2023, NAND manufacturers are exhibiting unprecedented capital and capacity discipline, which has now evolved into active strategic supply management. This is characterized by a dual strategy: controlling utilization and proactively managing output.

From Utilization Control to Active Output Reduction: In 2026, the two dominant suppliers, Samsung and SK Hynix (collectively holding >60% market share), are forecast to strategically reduce NAND wafer starts. Samsung's output is expected to decrease, with similar cuts from SK Hynix. This deliberate curtailment accelerates the industry's pivot towards higher-margin QLC technology for AI and solidifies pricing power.

Profitability Over Market Share: This move marks a definitive shift from chasing volume to prioritizing sustainable returns. By reducing output even amid strong demand, leaders aim to establish a permanently higher profitability floor.

Direct Market Impact: This calculated supply reduction is a primary driver behind the forecasted 33-38% quarterly surge in NAND contract prices for Q1 2026. The cyclical inventory glut of the past has been eliminated, with channel inventories at historic lows (~4-6 weeks), making pricing acutely sensitive to any demand signal and amplifying the impact of AI-driven demand.

3.4 The 3D NAND Layer Race and Technological Bottlenecks

The technology roadmap is defined by the transition to higher 3D stack layers, a path marked by increasing technical complexity and capital intensity.

Roadmap to 400+ Layers: The industry is accelerating toward 400+ layer production, a milestone critical for achieving the continued cost-per-bit reductions required for AI-scale storage. All major manufacturers are engaged in intense competition to advance their respective roadmaps.

The Hybrid Bonding Hurdle: Scaling beyond approximately 500 layers necessitates a pivotal shift from Through-Silicon Via (TSV) to Hybrid Bonding (e.g., Cu-Cu bonding). This transition introduces significant new challenges in process complexity, thermal management, and yield control. It raises the structural cost floor for advanced NAND production and acts as a significant barrier to entry, consolidating cutting-edge manufacturing among a few leading players.

QLC/PLC for Density: To maximize storage density for bulk data, the industry is rapidly adopting Quad-Level Cell (QLC) technology in enterprise segments and actively developing Penta-Level Cell (PLC). This highlights the focus on achieving optimal capacity per unit area for AI data lakes.

3.5 Evolving Competitive Landscape and Strategic Segmentation

The competitive landscape is stratifying in response to technological hurdles and evolving market demand, leading to increased specialization.

Incumbent Focus on High-Margin Segments: Established leaders are strategically concentrating on the high-performance, high-capacity enterprise and AI-driven markets. Their focus on technology leadership and supply control in these segments secures stronger pricing power.

Rise of Chinese Competition: Yangtze Memory Technologies Corp. (YMTC) has steadily increased production and technological capability. Its growing presence exerts competitive pressure in mainstream consumer and client SSD segments.

Market Specialization: This dynamic is fostering a more tiered market structure. Incumbents solidify their hold on the premium "AI storage" segment, while other competitors focus on volume-driven, mainstream markets.

Table 2: Strategic Focus of Leading NAND Flash Suppliers

Supplier	Technology & Capacity Focus	Key Product/ Market Strategy
Samsung	Leadership in high-layer (430+) V-NAND; broad TLC portfolio.	Dominates mainstream enterprise SSD market with a full portfolio.
SK Hynix Solidigm	Aggressive QLC capacity ramp; focus on high-density storage.	Leader in high-capacity QLC SSDs for AI data lakes and HDD replacement.
Micron	Advancing 200+ layer production; competitive SSD products.	Gains market share through competitive PCIe Gen4/Gen5 SSD offerings.
Kioxia WDC	Pursuit of high-layer technology; flexible supply model.	Supplies both finished SSDs and NAND components to CSPs.
YMTC	Rapid scaling of Xtacking 3.0 (200+ layer) production.	Focuses on consumer and entry-level enterprise segments.

Source: TrendForce, Gartner, Counterpoint Research

3.6 Price Trends and Market Outlook

The interaction of structural demand and managed supply is directly reflected in market pricing and forward-looking projections.

Price Forecast: As detailed in the report's macro section (Figure 1-1), industry consensus forecasts significant NAND contract price increases through 2026. Major analyst firm TrendForce projects Q1 2026 price growth of 55-60% quarter-over-quarter (QoQ), with full-year 2026 growth estimated at 105-110%. Price increases are anticipated to moderate sequentially throughout the year.

Supply-Demand Balance: Based on current trends of disciplined supply expansion and sustained demand growth, analysts project the storage market could approach a supply-demand balance in the first half of 2027.

Table 3: Comparative Analysis: DRAM vs. NAND in the AI Supercycle

Characteristic	DRAM/HBM Market	NAND Flash Market
Primary AI Driver	Real-time compute: Feeding data to GPU/TPU cores.Mark	Data pipeline: Storing training datasets, model checkpointsOtto
Key Demand Product	High-Bandwidth Memory (HBM), DDR5 RDIMMsJacob	High-Capacity Enterprise SSDs (eSSDs), especially QLC.
Core Constraint	“AI Tax” on advanced wafer capacity; TSV/stacking complexity.	Manufacturing discipline (controlled utilization); controller supply.
Technology Roadmap	Moving to HBM4 (16-high stacks); DDR6 development.	Racing to 400+ 3D NAND layers; adoption of hybrid bonding.the Bird
Pricing Power Driver	Allocation-based; 100% LTA sell-out for HBM.	Supply-controlled; disciplined capacity expansion.

Source: TrendForce, Gartner, Yole

04

The Memory Power
Shift: Strategic
Positioning in a
Geopolitically
Fractured Market

4. The Memory Power Shift: Strategic Positioning in a Geopolitically Fractured Market

4.1 Major Manufacturer Strategic Positioning

4.1.1 Samsung Electronics: The Catch-Up Strategy

Samsung entered 2025 in a vulnerable position, having fallen behind SK Hynix in the HBM market despite being the historical memory industry leader. The company is now executing an aggressive recovery plan.

Capacity Expansion: Samsung is expanding its Pyeongtaek P4 and P5 fabs in South Korea, along with its Taylor, Texas facility in the United States. The strategic goal is to increase HBM capacity by more than 2.5 times the 2025 level by 2026, with HBM4 becoming the dominant focus.

Critical Challenges: Samsung faces yield issues with its 1c nm DRAM process, which have become a persistent problem. These yield challenges could affect the on-time delivery of HBM4 products. Additionally, Samsung is among the most aggressive of the three major manufacturers in reducing DDR4 capacity, which has directly contributed to turbulence in the DDR4 market.

4.1.2 SK Hynix: The Market Leader

SK Hynix holds the strongest position in AI memory markets, leveraging its first-mover advantage in HBM3e technology.

Strategic Advantage: The company currently dominates with long-term supply agreements secured with major customers like NVIDIA, Google, and Meta. SK Hynix has established a close alliance with TSMC, leveraging TSMC's CoWoS packaging technology to enhance HBM system integration. This "powerful collaboration" has created very high competitive barriers that competitors struggle to overcome.

Expansion Plans: To consolidate its advantage, SK Hynix is accelerating construction of the M15X fab in Cheongju, South Korea. This facility is positioned as the core production base for HBM4 and HBM4E, with production expected to start in 2026. The Yongin semiconductor cluster is also under development as a longer-term plan for 2027 and beyond.

4.1.3 Micron Technology: Value Over Volume

Micron has adopted a financially driven strategy of "value over scale," choosing not to pursue market share blindly.

Geographic Strategy: Micron is building large-scale fabs in the United States specifically in Boise, Idaho and Clay, New York—leveraging subsidies from the CHIPS Act. However, this new capacity will not be available at scale until after 2027. In the short term, Micron is supporting HBM production by upgrading its existing factories in Taiwan and Japan.

Product Strategy: Micron has announced its exit from certain low-margin consumer memory businesses, including some Crucial retail products. The company is focusing resources on data center and automotive markets. This strategy has intensified supply tightness in the consumer market.

4.1.4 Kioxia and SanDisk: The NAND Duopoly

Corporate Restructuring: Western Digital completed its spin-off in 2024, with its flash memory business now operating independently as SanDisk Corporation (NASDAQ ticker: SNDK). Meanwhile, Kioxia completed its IPO on the Tokyo Stock Exchange in December 2024.

Joint Venture Structure: Despite the corporate separation, their manufacturing joint ventures remain stable. Kioxia holds roughly 60% of the production capacity, while SanDisk holds 40%. Together, they operate fabs in Yokkaichi and Kitakami, Japan.

Kitakami Fab 2 - The Critical Expansion: The Kitakami Fab 2 is expected to be the engine of future growth for both companies, focusing on BiCS8 (218-layer) and BiCS10 (332-layer) 3D NAND production. The fab is projected to enter its ramp-up phase in the first half of 2026, providing key incremental capacity for AI storage applications.

Merger Speculation: With Kioxia now publicly listed and SanDisk independent, merger discussions have resurfaced. If successful, the combined entity could rival Samsung in NAND bit output, further increasing industry concentration and bargaining power.

4.2 Alternative Suppliers: Filling Market Gaps

4.2.1 Nanya Technology

As the world's fourth-largest DRAM manufacturer, Nanya Technology is transitioning from DDR3/DDR4 to DDR5, though this process will take time. With the three major global players exiting the DDR4 market, Nanya has become a key alternative supplier, giving it stronger pricing power. The company has consecutively raised DDR4 contract prices throughout 2025. Nanya represents an important secondary source for DDR4 and mainstream DDR5, particularly for customers seeking to reduce dependence on the Big Three manufacturers.

4.2.2 Winbond and Macronix

Winbond is focused on NOR Flash and niche DRAM products. The company is set to benefit from rising demand for NOR Flash in automotive electronics and IoT devices, such as ADAS systems. Both Winbond and Macronix have exercised significant pricing power. Macronix has reportedly raised NOR Flash prices by 30% for Q1 2026, while Winbond has implemented similar increases in Q4 2025. These specialty memory suppliers serve automotive, industrial, and IoT markets where long product lifecycles and high reliability are more important than cutting-edge performance.

4.3 Geopolitical Risks and Supply Chain Vulnerabilities

4.3.1 U.S.-China Technology Decoupling

The Containment Strategy

The U.S. containment strategy targeting China's semiconductor industry is expected to intensify further in 2025-2026. Beyond controls on exports of advanced equipment, the use of tools such as the "1260H List" increases legal risks across the supply chain.

The Dual-Track Market

Chinese manufacturers are rapidly expanding capacity but much of this output is effectively "isolated" from the global free-flowing market due to sanctions and compliance concerns. This creates overcapacity within China while the rest of the world faces continued supply tightness a dual-track market scenario.

The result is a bifurcated market where:

- Western/Allied markets face severe shortages and premium pricing
- Chinese domestic market has adequate supply for mature products at competitive prices
- Global buyers must navigate complex compliance requirements when sourcing

4.3.2 Geographic Concentration Risks

Taiwan Vulnerabilities

Taiwan hosts critical memory manufacturing capacity but faces multiple risk factors:

- Seismic Risk: An earthquake in Taiwan in early 2025, although causing no structural damage, led to the automatic shutdown of some sensitive lithography equipment, affecting the output of tens of thousands of wafers. Taiwan experiences frequent seismic activity due to its location on the Pacific Ring of Fire.

- **Power Supply:** Instability in northern Taiwan's power grid, such as the 2024 blackout, poses potential risks to Micron and Nanya Technology facilities.
- **Geopolitical Tension:** Taiwan's geopolitical status creates potential supply chain disruption risks that buyers must consider in their risk planning.

Japan Risks

The memory industry supply chain is highly concentrated in earthquake prone regions. Any seismic activity in Japan (Kioxia, Micron's Hiroshima fab) could trigger global disruptions. Samsung and SK Hynix are both headquartered in South Korea with the majority of their production capacity concentrated there, creating geographic concentration risk despite the region's relative stability.

05

How to Position Your Organization for Supply Continuity

5. How to Position Your Organization for Supply Continuity

5.1 Executive Market Intelligence Summary

The 2025–2027 global storage and memory market is entering a structurally constrained super cycle, defined not by demand recovery alone but by supply reallocation toward AI-centric products. Market evidence indicates that conventional procurement and pricing models—historically reliant on cyclical oversupply—are no longer effective in this environment.

From a market intelligence standpoint, the period from 1H 2026 through 2027 represents a prolonged seller-advantaged phase, where capacity ownership, allocation priority, and design flexibility become the primary determinants of competitive positioning rather than unit cost optimization.

5.2 Supply Demand Intelligence Outlook

5.2.1 1H 2026: Peak Constraint Window

Market intelligence from TrendForce, IDC, and industry disclosures converges on 1H 2026 as the most supply-constrained interval within the forecast horizon:

- Channel inventories are expected to be largely depleted.
- New production capacity, including Kioxia's Fab2, will not yet be fully effective.
- DRAM and NAND shortages will be broad-based rather than node-specific.

Simultaneously, manufacturers continue to divert wafer capacity toward HBM and AI-optimized memory, tightening availability for PC DRAM, server DRAM, and enterprise SSD components.

During this phase, supply access becomes a strategic asset. Buyers without secured allocation face heightened risks of shipment delays, forced configuration downgrades and margin compression.

5.2.2 2H 2026: Controlled Easing Without Price Normalization

While limited supply relief may emerge in the second half of 2026 driven by incremental HBM capacity release and yield improvements market intelligence indicates that price normalization is unlikely:

- NAND manufacturers maintain disciplined output control to preserve pricing power.
- DRAM suppliers continue prioritizing higher-margin AI products.

The market transitions from acute shortage to structural tightness, establishing a new elevated price floor rather than triggering a downcycle.

5.2.3 2027: Demand-Absorbed Rebalancing

The commissioning of new fabs by Micron and Samsung may narrow the supply-demand gap in 2027. However:

- AI PC and AI smartphone upgrade cycles introduce incremental demand.
- Server memory density requirements continue to rise. As a result, intelligence forecasts suggest price stability at elevated levels, rather than a rapid correction.

Supply growth is likely to be absorbed by new demand vectors, limiting downside pricing risk.

5.3 Price Intelligence: Indexed Trend Analysis

Indexed to Q4 2025 = 100, all major storage and memory categories demonstrate persistent upward pricing momentum throughout 2026:

Product Category	2026 Q1	2026 Q2	2026 Q3	2026 Q4	Primary Intelligence Driver
PC DRAM (DDR5)	115-120	125-130	130-135	135-140	HBM capacity crowd-out + AI PC adoption
Server DRAM	120-125	130-140	145-150	150+	AI server memory density escalation
DDR4 (Legacy)	110-115	120-125	125-130	130	Accelerated capacity phase-out
Enterprise SSD	115-120	125-135	135-145	145-150	AI data lake demand + controller shortages
NAND Flash Wafer	110	115	120	120-125	Output discipline + cautious CAPEX
LPDDR5X	150	120	125	130	Mobile AI capacity competition

Sources: TrendForce, IDC, Gartner

5.4 Strategic Procurement Intelligence Responses

5.4.1 Short-Term (Next 3–6 Months): Defensive Positioning

Long-Term Agreement (LTA) Acceleration: Intelligence indicates that early commitment is essential as significant portions of 2026 output are already allocated. Capacity assurance should supersede price concessions

Pre-emptive Inventory Buffering: Establishing 3–6 months of buffer inventory ahead of 1H 2026 materially reduces exposure to peak pricing volatility and allocation risk.

Cost Baseline Reset: A 20–30% upward adjustment in 2026 storage BOM budgets is necessary to reflect market realities and avoid reactive downstream pricing actions.

5.4.2 Mid-Term (2026–2027): Structural Risk Mitigation

Supplier Portfolio Intelligence

Legacy DRAM

As tier-1 memory suppliers accelerate the phase out of legacy and long life DRAM, supply continuity risks are rising for industrial and networking applications. Second-tier specialty DRAM vendors are expected to play an increasingly important role in maintaining long-lifecycle support.

Client SSD

While NAND suppliers continue to expand capacity, client SSD supply remains subject to allocation bias toward AI and enterprise segments. Market participants are therefore expected to broaden supplier portfolios to reduce single supplier exposure and improve supply resilience.

Conclusion

The 2025–2027 memory market will be a battle over resource allocation rather than pure cost competition. The rise of AI is not only reshaping computing architectures, but also redefining how capacity, pricing power, and value are distributed across the semiconductor supply chain. For the electronics manufacturing industry, this environment presents both a sustained cost challenge and a direct test of supply chain management capability. Only organizations that can anticipate market inflection points, make timely and decisive procurement commitments, and build resilient, diversified supply chains will be positioned to navigate this cycle with minimal disruption. If you would like to discuss how these dynamics may impact your organization's sourcing strategy, please reach out to our team via email marketing@briocean.com to start a confidential conversation or visit our website www.briocean.com

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